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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RICHARDS, N DREW	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/876,554	Applicant(s) IIDA, IZUO	
	Examiner N. Drew Richards	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-18* is/are pending in the application.

4a) Of the above claim(s) *4-10,17 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 11-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. In applicants amendment filed 9/23/03 claim 16 has been amended in response to the rejection under 35 U.S.C. 112, first paragraph. Upon further review of the application, the examiner has determined that the previous 35 U.S.C. 112, first paragraph rejection was improper as the specification did enable the "selectively etching the tunnel insulating film on the region of the semiconductor substrate where the MOS transistor is to be formed." See specification page 11 lines 11-14. Thus, the examiner acknowledges that claim 16 as originally presented met the requirements of 35 U.S.C. 112, first paragraph. However, claim 16 as currently amended does raise issues of new matter and will be treated accordingly below. For the sake of art rejections, the examiner will consider claim 16 as originally presented and supported by the specification such that a proper determination of it's patentability over the prior art can be achieved.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 16 as currently amended is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 16 as currently amended recites the limitation "selectively etching the tunnel insulating film **except from** on the region of the semiconductor substrate where the MOS transistor is to be formed." This limitation was not described in the specification as originally filed. As can be seen in figure 6, the tunnel insulator 16 is not etched in the region of the memory cell but instead remains between the floating gate 14 and the control gate 17. Though not explicitly labeled, it appears that the tunnel insulator 16 remains on most portions of the substrate.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3 and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komori et al. (U.S. Patent No. 5,656,522) in view of Hsieh et al. (U.S. Patent No. 6,165,845).

Komori et al. teaches in figure 4 and on column 5 lines 34-36 and column 8 lines 23-33, a method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, the method comprising

simultaneously forming the oxide film 8 on the floating gate 7a of the non-volatile memory cell transistor and a gate insulating film 8 of the MOS transistor in a single thermal oxidation step. Komori et al. does not teach selectively forming the oxide film on the floating gate.

Hsieh et al. teach a method of fabricating a poly tip in a split-gate flash EEPROM memory cell. Hsieh et al. teach selectively forming the oxide on the floating gate in figure 3f.

Komori et al. and Hsieh et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to selectively form the oxide film on the floating gate. The motivation for doing so is to provide a gate bird's beak to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell. Therefore, it would have been obvious to combine Komori et al. with Hsieh et al. to obtain the invention of claim 1.

With regard to claim 11, Komori et al. teach a method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate. Specifically, Komori et al. teach forming a silicon layer 7a on the substrate 1 (figure 3, column 8 lines 9-21), selectively removing the silicon layer on a region of the substrate where the MOS transistor is to be formed (figure 3, column 8 lines 9-21), and simultaneously forming an oxide film 8 on the region where the floating gate is to be formed and a gate insulating film 8 on the region where the MOS transistor

is to be formed (figure 4). Komori et al. do not teach forming an oxidation-resistant film over a first entire resulting surface, selectively removing the oxidation resistant film on the region of the substrate where the MOS transistor is to be formed and on a region of the substrate where the floating gate of the non-volatile memory cell transistor is to be formed, selectively forming the oxide film on the region where the floating gate is to be formed, or forming a tunneling insulating film over the gate insulating film.

Hsieh et al. teach a method of fabricating a poly tip in a split-gate flash EEPROM memory cell. Hsieh et al. teach forming an oxidation resistant film 50 over a first entire surface (figure 2b) and selectively removing the oxidation-resistant layer on the region where the floating gate of the non-volatile memory cell transistor is to be formed (figure 2c). Hsieh et al. then teach selectively forming an oxide film 45 on the region where the floating gate is to be formed (figure 2d) and forming a tunneling insulating film 50 over the gate insulating film 45 (figure 2f). In combining the two references, it would be obvious to one of ordinary skill in the art a the time of the invention that the oxidation resistant film would be selectively removed on the region where the gate insulating film of the MOS transistor is to be formed as the process of Komori et al. teach forming the oxide on the floating gate and the gate insulating film of the MOS transistor in the same oxidation step.

Komori et al. and Hsieh et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an oxidation resistant film on the entire surface and selectively remove the oxidation-resistant film where the floating gate is to be formed

and where the MOS transistor is to be formed, to selectively form the oxide where the floating gate is to be formed, and to form a tunneling insulator over the gate insulating film. The motivation for doing so is to provide a gate bird's beak on the floating gate to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell and to form the tunneling insulator to insulate the control gate from the floating gate. Therefore, it would have been obvious to combine Komori et al. with Hsieh et al. to obtain the invention of claim 11.

With regard to claim 3, the oxidation resistant film of Hsieh et al. is taught as a silicon nitride film.

With regard to claim 12, the oxide film is formed by a single thermal oxidation step as taught by Komori et al.

With regard to claim 13, Komori et al. teach a method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate. Specifically, Komori et al. teach forming a first gate insulating film 6 on the semiconductor substrate 1 (figure 2), forming a silicon layer 7a on the first gate insulating film 6 (figure 3, column 8 lines 9-21), selectively removing the silicon layer on a region of the substrate where the MOS transistor is to be formed (figure 3, column 8 lines 9-21), and simultaneously forming an oxide film 8 on the region where the floating gate is to be formed and a second gate insulating film 8 on the region where the MOS transistor is to be formed (figure 4). Komori et al. do not teach forming an

oxidation-resistant film over a first entire resulting surface, selectively removing the oxidation resistant film on the region of the substrate where the MOS transistor is to be formed and on a region of the substrate where the floating gate of the non-volatile memory cell transistor is to be formed, selectively forming the oxide film on the region where the floating gate is to be formed, removing at least some of the remaining oxidation-resistant film, or forming a tunneling insulating film over the gate insulating film.

Hsieh et al. teach a method of fabricating a poly tip in a split-gate flash EEPROM memory cell. Hsieh et al. teach forming an oxidation resistant film 50 over a first entire surface (figure 2b) and selectively removing the oxidation-resistant layer on the region where the floating gate of the non-volatile memory cell transistor is to be formed (figure 2c). Hsieh et al. then teach selectively forming an oxide film 45 on the region where the floating gate is to be formed (figure 2d), removing at least some of the remaining oxidation-resistant film (figure 2e) and forming a tunneling insulating film 50 over the gate insulating film 45 (figure 2f). In combining the two references, it would be obvious to one of ordinary skill in the art a the time of the invention that the oxidation resistant film would be selectively removed on the region where the gate insulating film of the MOS transistor is to be formed as the process of Komori et al. teach forming the oxide on the floating gate and the gate insulating film of the MOS transistor in the same oxidation step.

Komori et al. and Hsieh et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of

ordinary skill in the art to form an oxidation resistant film on the entire surface, selectively remove the oxidation-resistant film where the floating gate is to be formed and where the MOS transistor is to be formed, selectively form the oxide where the floating gate is to be formed, remove at least some of the remaining oxidation-resistant film, and form a tunneling insulator over the gate insulating film. The motivation for doing so is to provide a gate bird's beak on the floating gate to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell and to form the tunneling insulator to insulate the control gate from the floating gate. Therefore, it would have been obvious to combine Komori et al. with Hsieh et al. to obtain the invention of claim 13.

With regard to claim 14, the oxidation-resistant film of Hsieh et al. is taught as a silicon nitride film.

With regard to claim 15, the oxide film is formed by a single thermal oxidation step as taught by Komori et al.

Allowable Subject Matter

6. Claim 16 as originally presented contains allowable subject matter and would be allowable if (1) rewritten in independent form including all of the limitations of the base claim and any intervening claims and (2) rewritten as originally presented.

7. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach, disclose, or suggest, either alone or in

combination, the process further including selectively etching the tunnel insulating film on the region of the semiconductor substrate where the MOS transistor is to be formed.

Response to Arguments

8. Applicant's arguments filed 9/23/03 have been fully considered but they are not persuasive.

Applicant argues that the combined teachings of Komori et al. with Hsieh et al. do not teach selectively forming a gate insulating film on the region where the MOS transistor is to be formed. This is not persuasvie because the combined references do teach this. Komori et al. teach simultaneously forming the oxide film on the floating gate and the gate insulating film of the MOS transistor. Hsieh et al. teach selectively forming the oxide film on the floating gate of the non-volatile memory cell tansistor by masking with a nitride and a photoresist mask. In combining the selective oxidation of Hsieh et al. with the simultaneous oxidation of Komori et al., one would form the nitride and photoresist masks such that they left the portion where the floating gate was to be formed and the region where the gate insulator was to be formed exposed so that the single oxidation step could still be used to simultaneously form both the oxide film and the gate intulating film. The oxidation step would then necessarily be selective to both the oxide film on the floating gate and the gate insulating film of the MOS transistor. With a mask applied over parts of the substrate, the oxidation that takes place in the unmasked portions is necessarily selective as it does not oxidize where the mask is applied.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NDR

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